Electronic Version
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Claims

[c1] What is claimed is:

1.A microprocessor system capable of software debug comprising:

a host computer for executing remote debug;

a program memory for storing a monitor program for proving monitoring of the host computer and a user program;

at least one break point address holder for temporarily storing a break point address from the host computer;

a break point comparator unit connected to the break point address holder for comparing the break point address from the break point address holder with an address of the user program being executed, and for outputting an interrupt control signal when the addresses match;

a controller for controlling the break point comparator unit; and

a microprocessor electrically connected to the host computer comprising:

a host interface connected to a transmit port of the host computer for transmitting signals between the microprocessor and the host computer;

a program memory address pointer for indicating an address of the program memory and outputting the address of the user program being executed to the break point comparator unit; and
an interrupt control unit for receiving the interrupt control signal from the break point comparator unit;
wherein when the interrupt control unit receives the interrupt control signal from the break point comparator unit, the microprocessor executes the monitor program in the program memory in order to transmit the status of execution of the user program to the host computer.

[c2] 2.The microprocessor system of claim 1, wherein the microprocessor system comprises two break point address holders, and the break point comparator unit comprises two break point comparators which receive and compare the break point addresses from the two break point address holders with the address of the user program being executed from the program memory address pointer; and the microprocessor system further comprises an interrupt generator for receiving signals of the two break point comparators, and outputting a corresponding interrupt control signal to the interrupt control unit.

[c3] 3.The microprocessor system of claim 1, further comprising a data memory for storing temporary data generated while executing the program.

[c4] 4.The microprocessor system of claim 3, wherein the microprocessor further comprises a data memory address pointer for indicating data in the data memory.

[c5] 5.The microprocessor system of claim 1, wherein the microprocessor further comprises a data access port for transmitting the break point address transmitted from the host computer to the break point address holder, and for transmitting a control signal to the controller.

[c6] 6.The microprocessor system of claim 1, wherein the host computer is a computer device.

[c7] 7.The microprocessor system of claim 1, wherein the program memory is a read-only memory.

[c8] 8.The microprocessor system of claim 1, wherein the program memory is a read/write memory.

[c9] 9.A method of software debug emulation comprising:
(a) executing a user program;
(b) comparing a break point address and an address of the user program being executed, and outputting an interrupt control signal if the break point address matches the address of the user program being executed; and
(c) stopping executing the user program and outputting the status of the user program when receiving the inter-

rupt control signal.

[c10] 10.The method of claim 9, wherein in step (c), when receiving the interrupt control signal, a monitor program is executed to output the status of the user program.

[c11] A device for implementing the method of claim 9.